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NORTHROP GRUMMAN

Integrated Photonic Spectrometer for Sustainable Land Imaging - Technology

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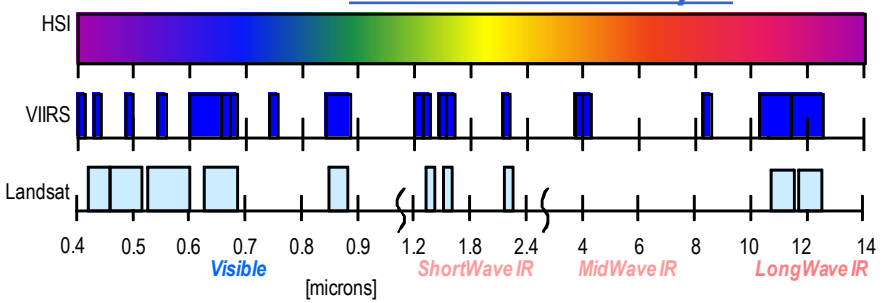
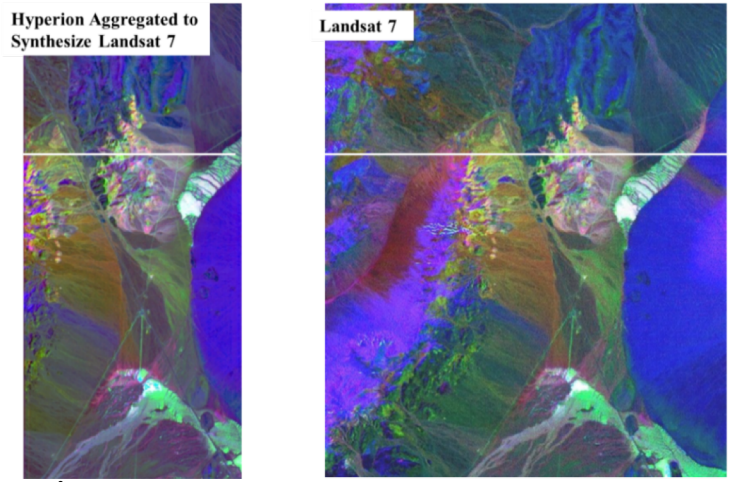
Hyperspectral Imaging

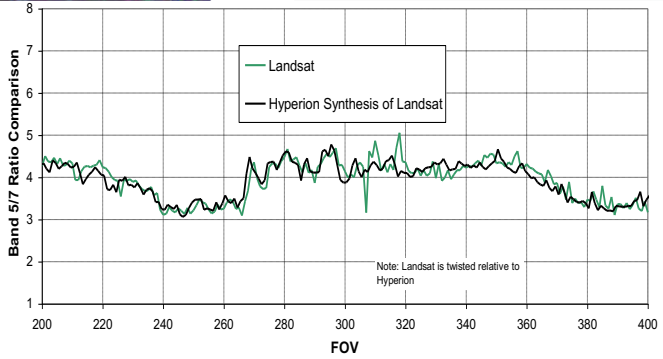
Hyperion VNIR/SWIR, Class D; less than 12 months to delivery; more than 16 years on orbit

Band-Selectable Output

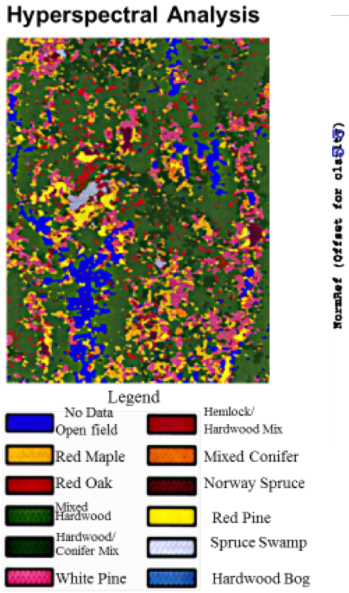


Mimic MSI through Band Aggregation

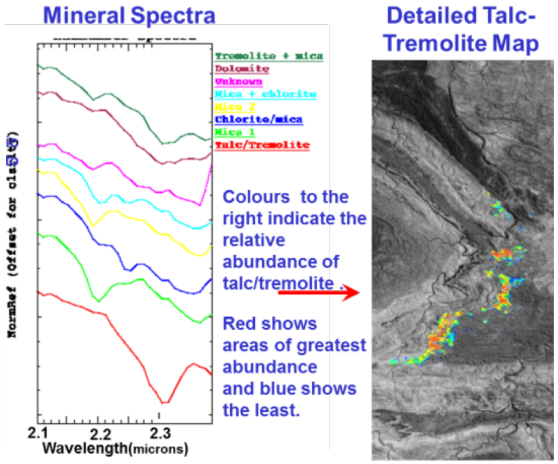




Full Hyperspectral Analysis



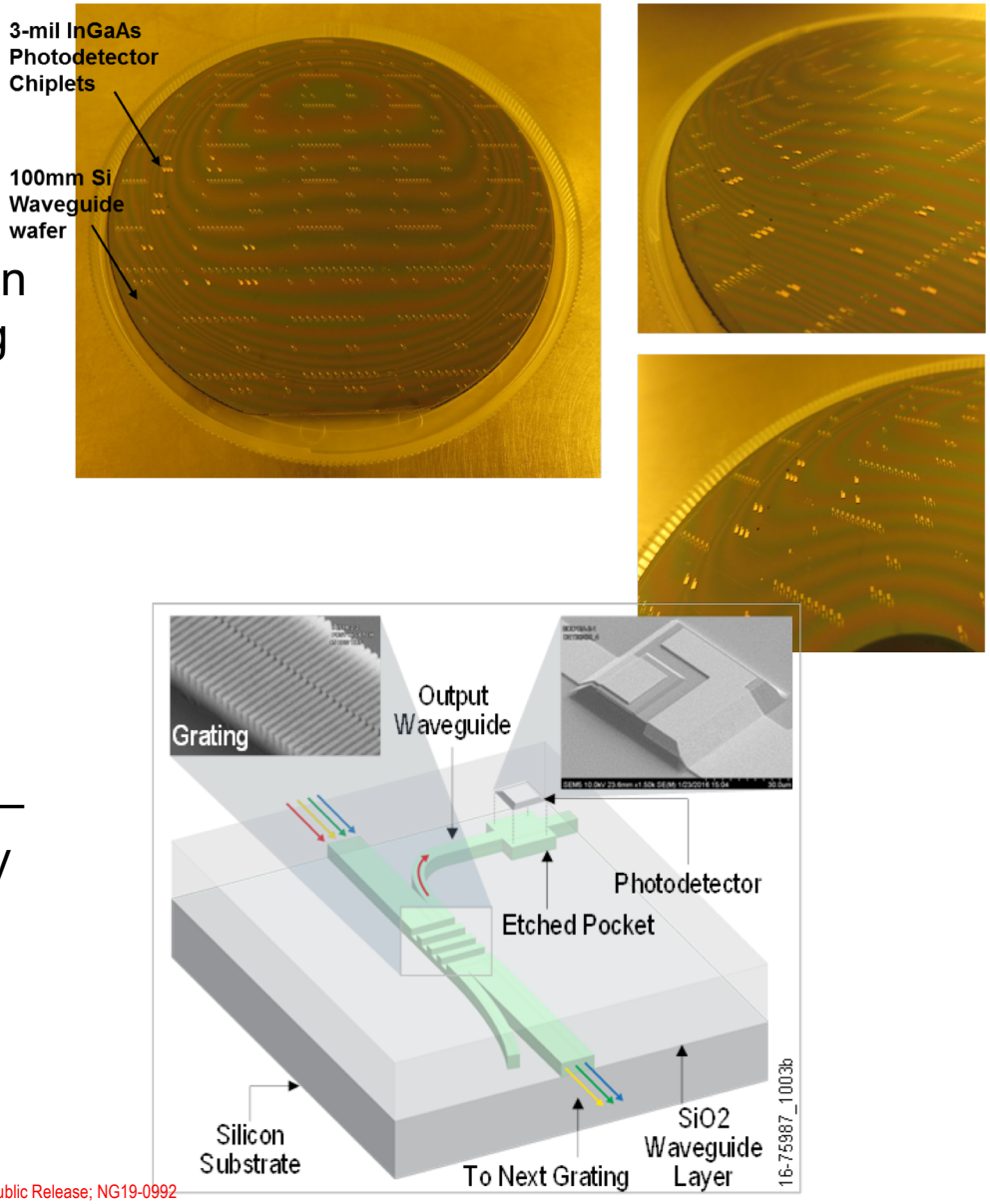
Analysis by Mary Martin University of New Hampshire



Courtesy of CSIRO, Australia

Photonic Integration Enables HSI Acquisition in an Extremely Compact Package

- Micro-fabricated photonic filters and integrated photodetectors replace free-space optics - enables sensor integration at microelectronic device scales yielding miniature instrument packages
- Integrated spectrometer manufacturing uses standardized, repeatable microelectronic processes – enables rapid and inexpensive patterning and reproduction
- Significantly reduces size of instrument – small enough to allow integration on any platform and along-side existing payloads (including shared apertures)



Sustainable Land Imaging –Technology Program

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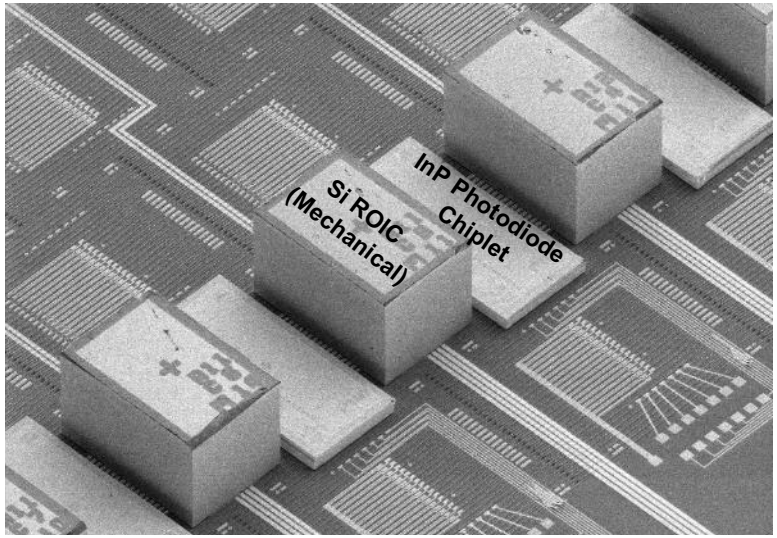
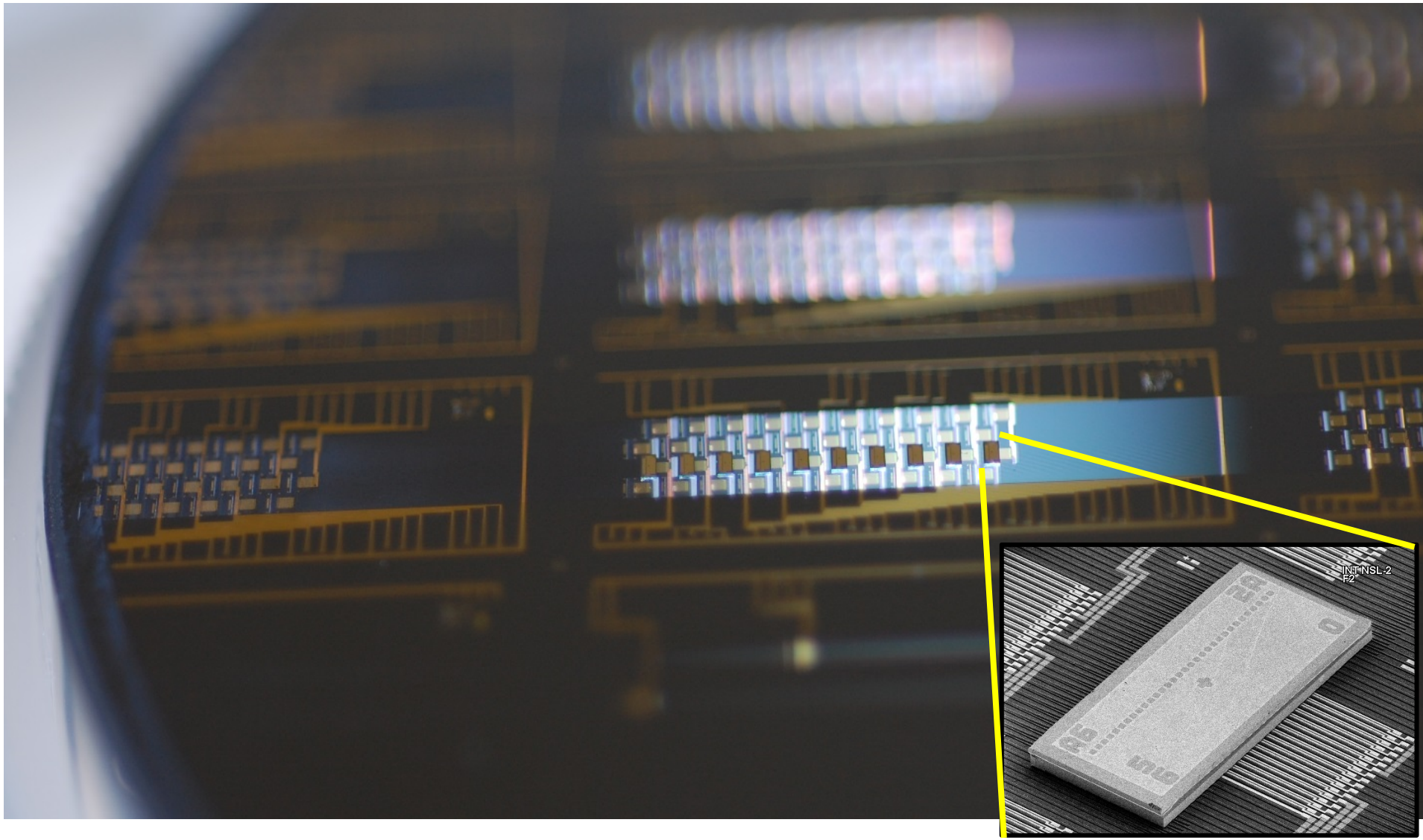
- NG is currently executing a 5-year development program funded by the NASA Earth Science Technology Office to build and test a heterogeneously integrated photonic instrument
  - Covers two SLI bands: Band 9 (1.36 – 1.39µm at 3nm resolution) and Band 6 (1.56 – 1.66µm at 6nm resolution). Demonstrating:
    - Scalability to SLI VNIR and SWIR bands
    - Integration of novel NG ROIC
    - Radiometric performance estimates and testing
- Planned exit TRL = 6 in September 2021

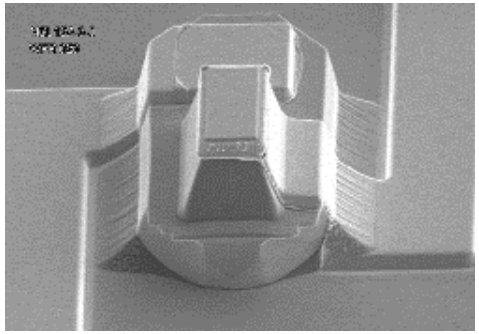


SWIR Integrated Photonic Spectrometer developed for NASA SLI-T (detail showing detectors and mechanical ROICs)

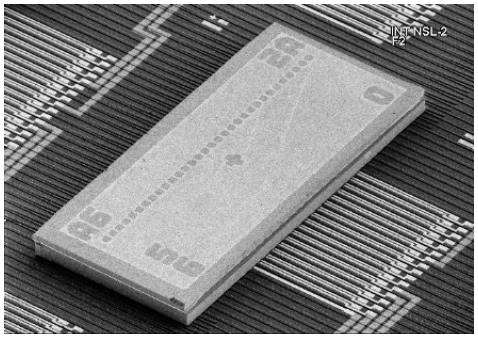
Full-Field Integration



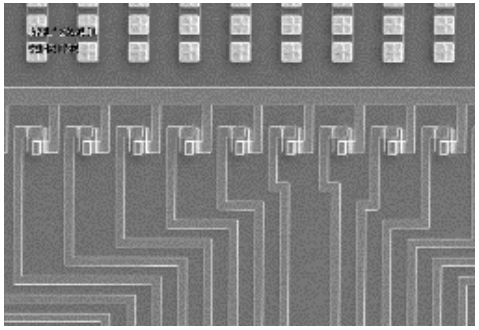
Detector Chiplet



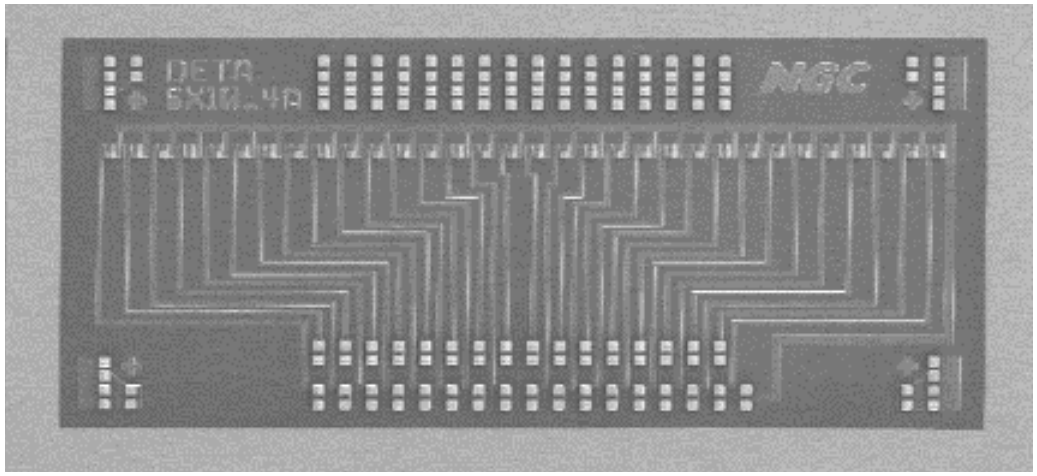
Detector array



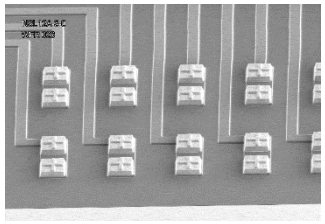
Chiplet backside



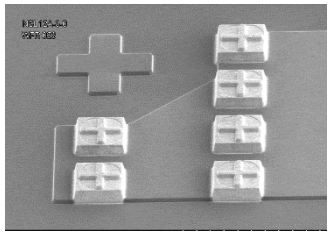
Interconnect traces



Chiplet frontside



Electrical Interconnects (eHICs)

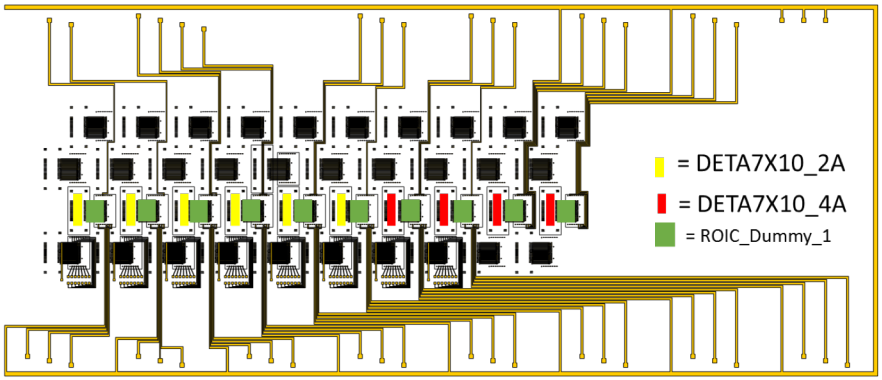


Structural tHICs

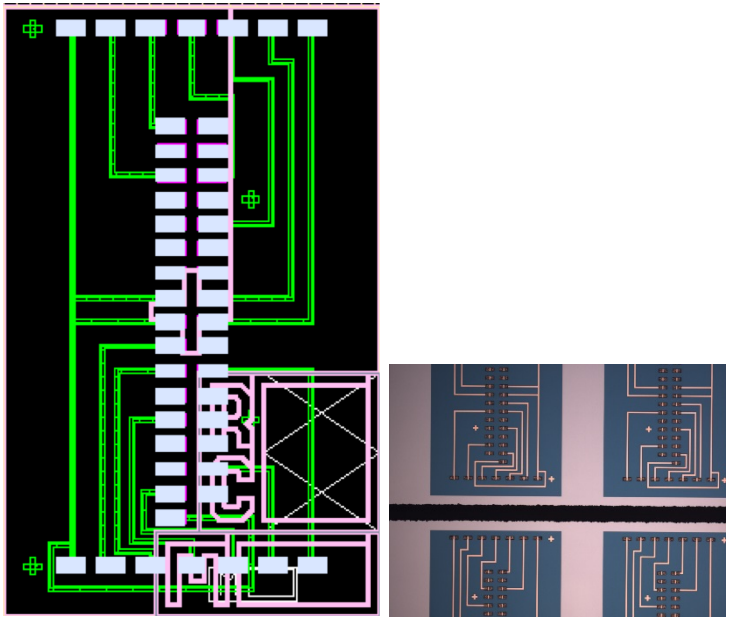
Detector – ROIC Integration

- Our integration processes have resulted in consistently high accuracy detector placement (within 0.2 µm) in the PLC

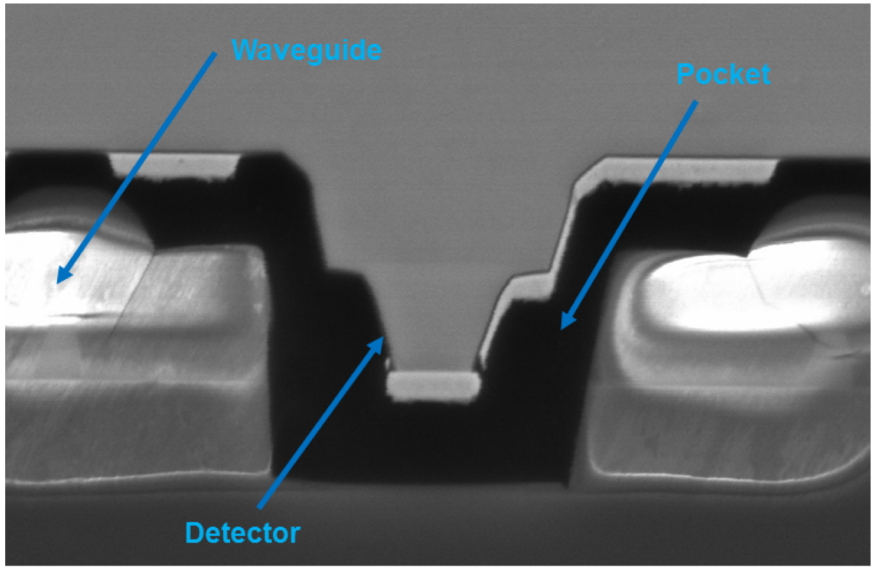
NSL1 Wafer Map-Integration Summary



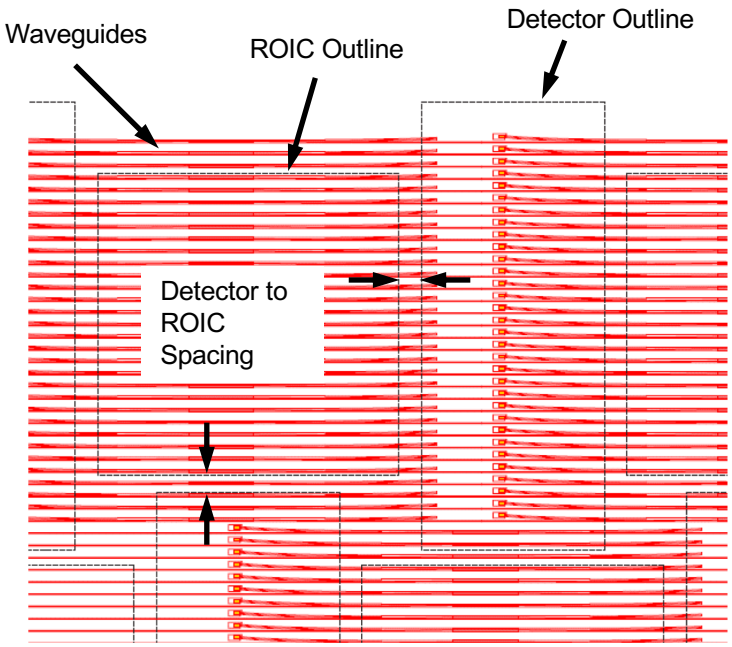
Mechanical ROIC Layout and Fab

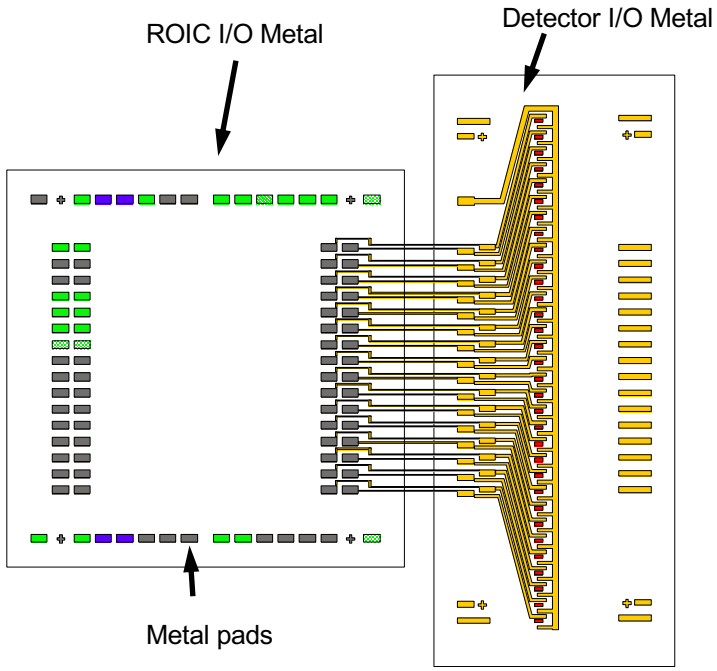


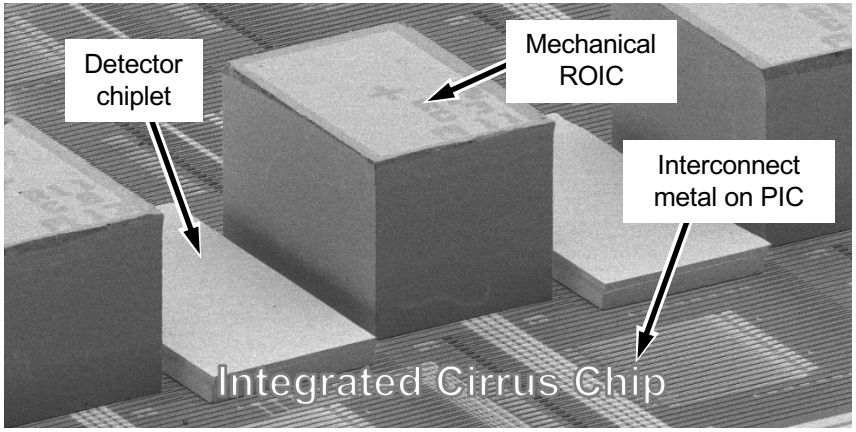
Detector to Waveguide Integration

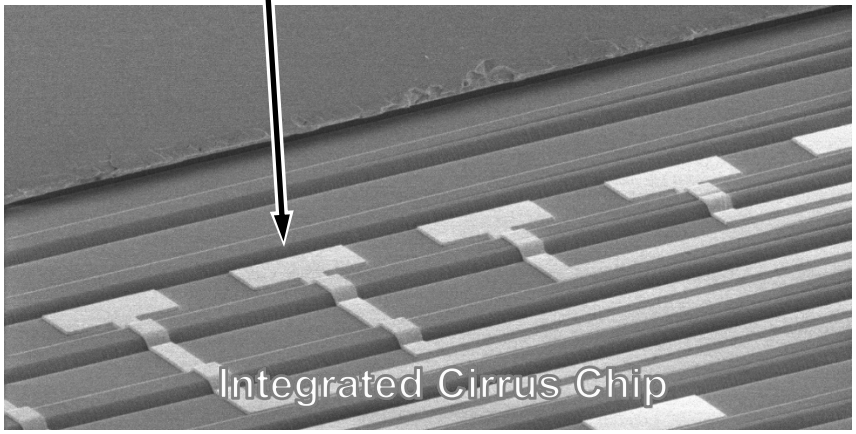


Integrated PIC – Detector – ROIC Configuration



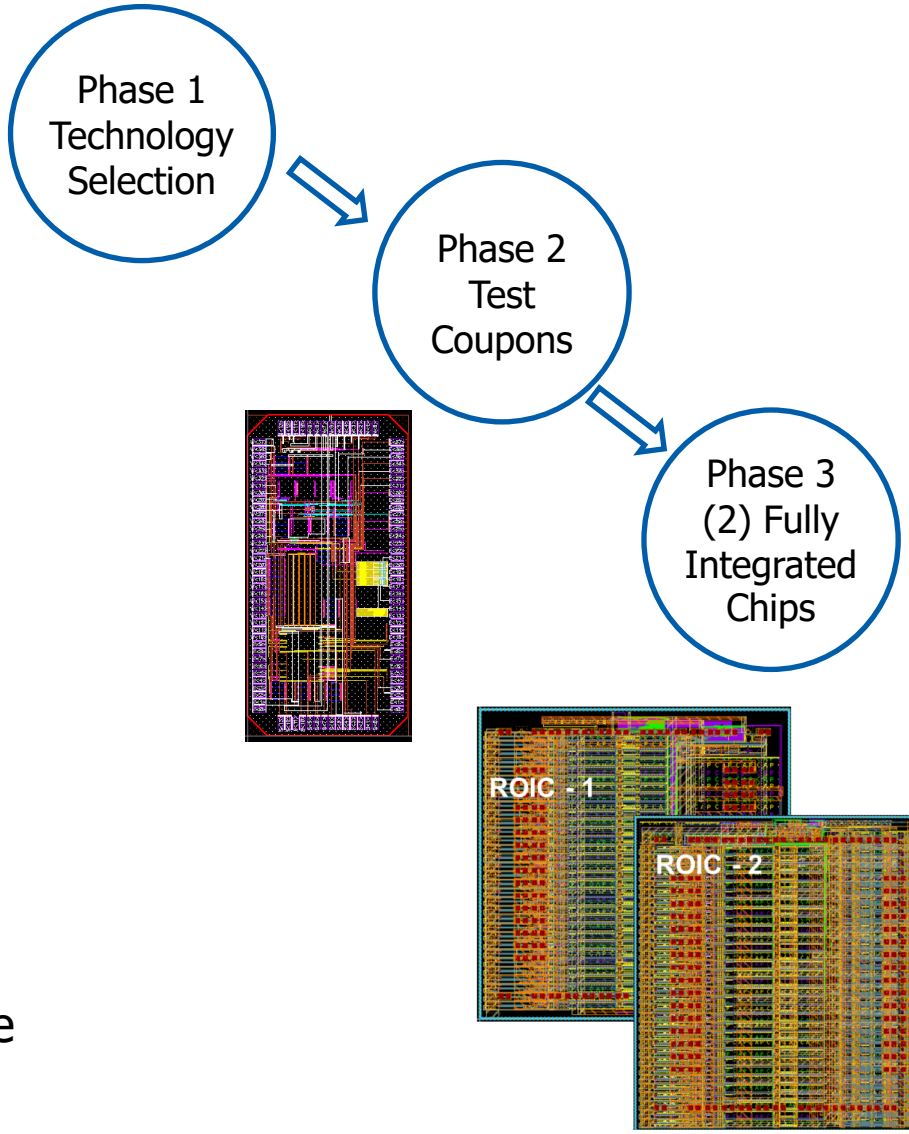






ROIC Development

- Program is developing custom CMOS digital Readout Integrated Circuit chiplets
- ROIC requirements derived from SLI-T system requirements and sensor-level radiometric performance estimates
- Designs optimized by trading signal to noise ratio and dynamic range against size, power, complexity, and risk
- Test coupons were fabricated containing unit cells with multiple architectures and component designs
- Unit cells were mounted on a custom break-out board for testing
- Actual and predicted ROIC performance were compared and designs optimized



Unit Cell Characterization Board

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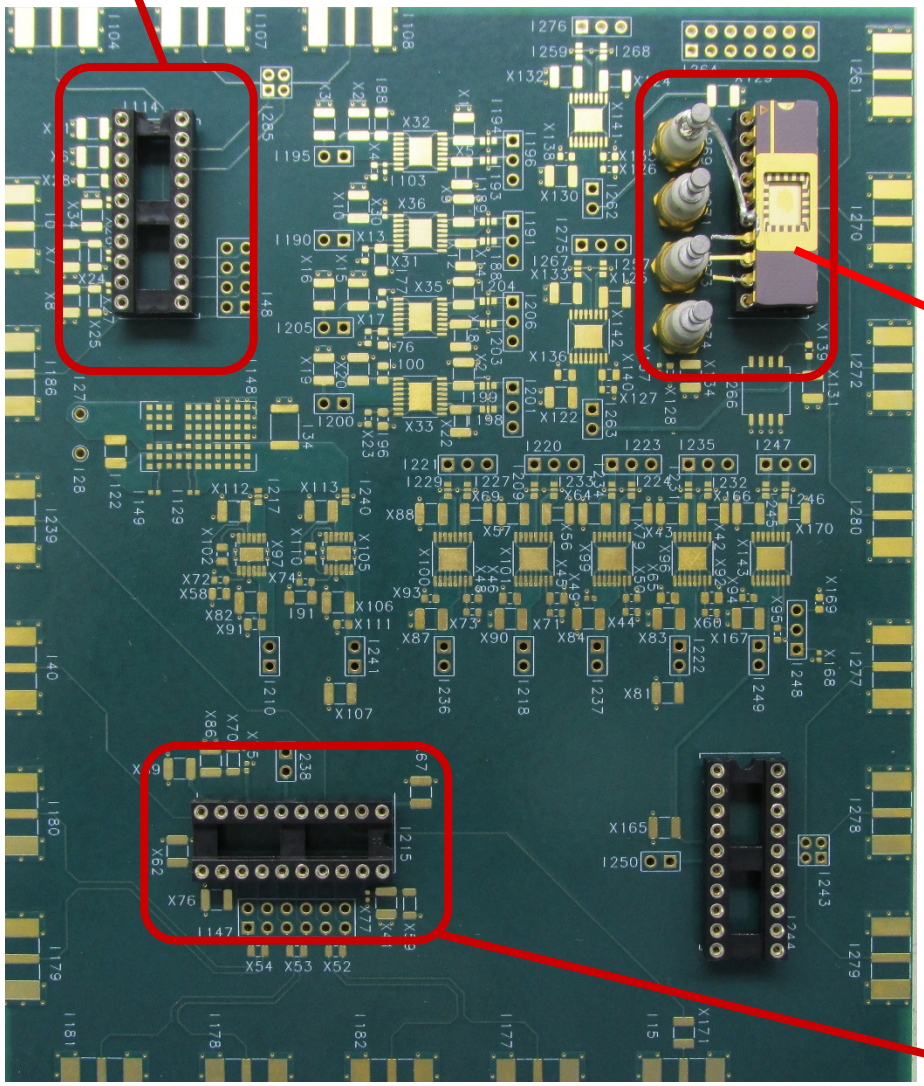
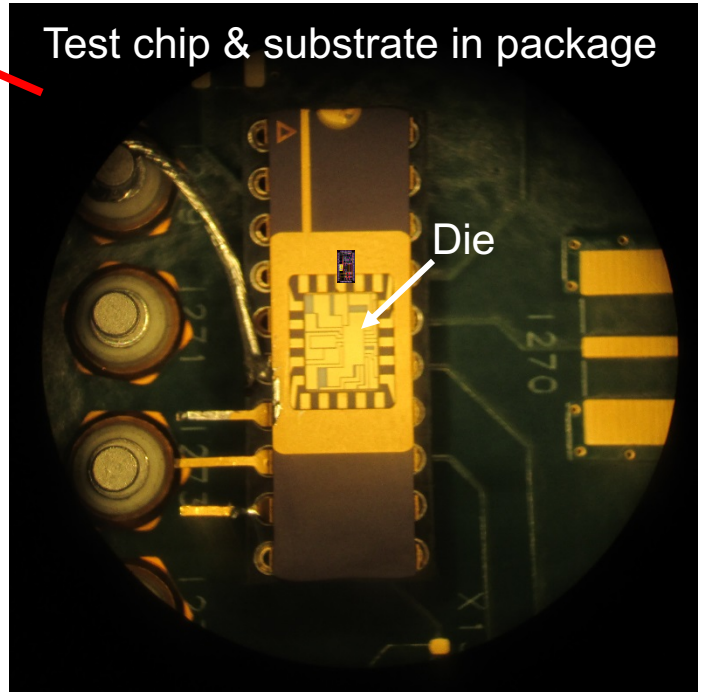
Design Variant #1 Test

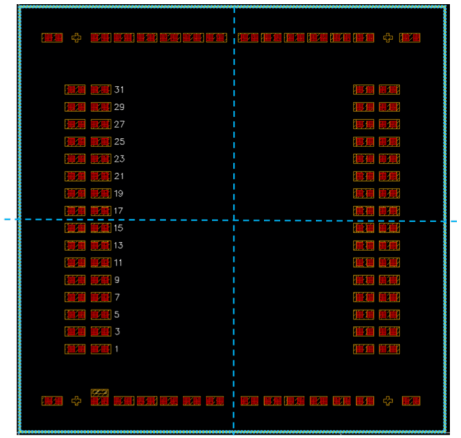




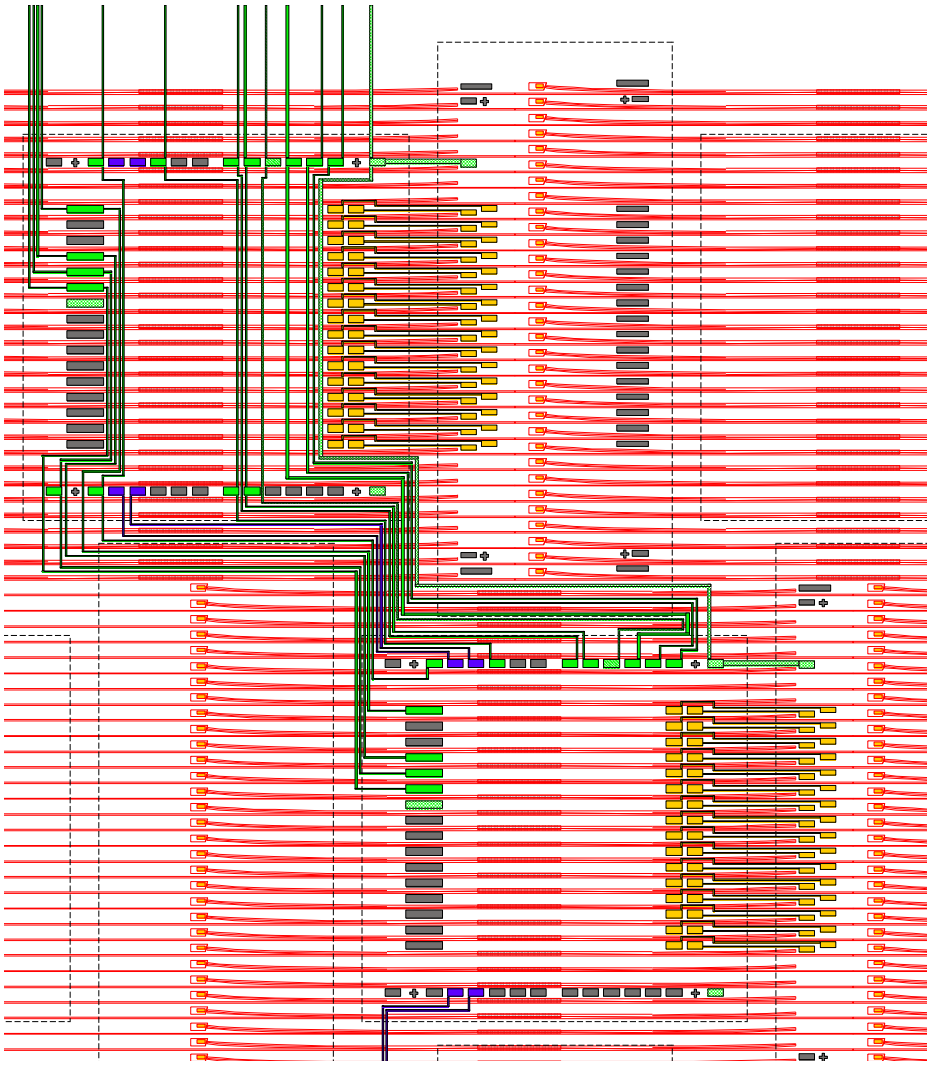
Design Variant #2 Test

ROIC Interconnect

ROIC Face Up: Common I/O for ROIC Variants



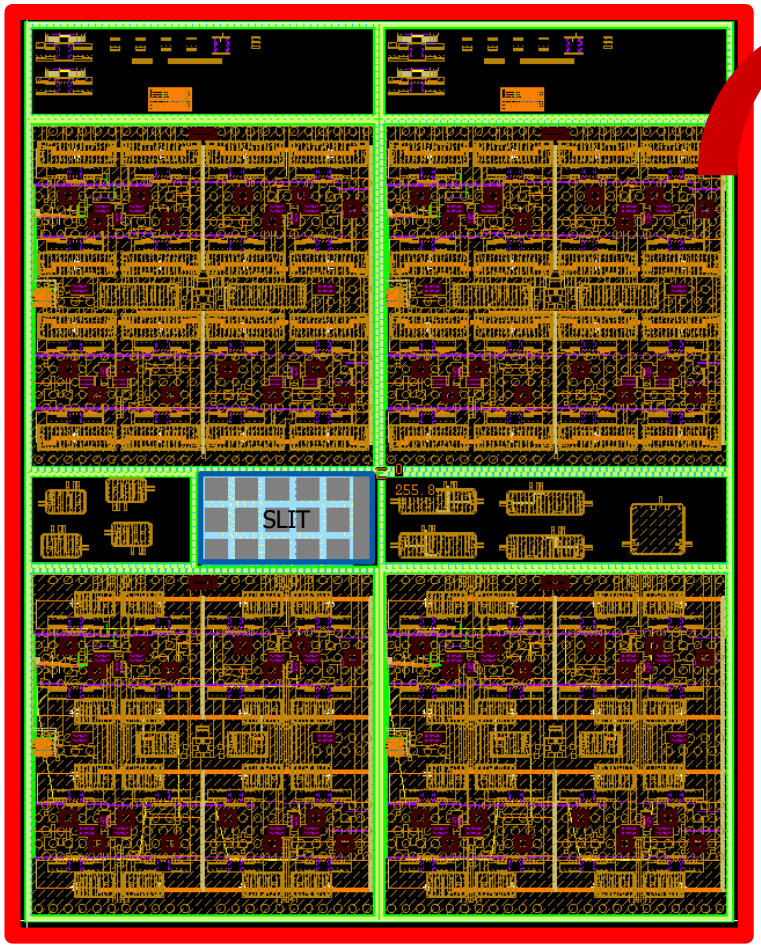
ROIC Interconnection

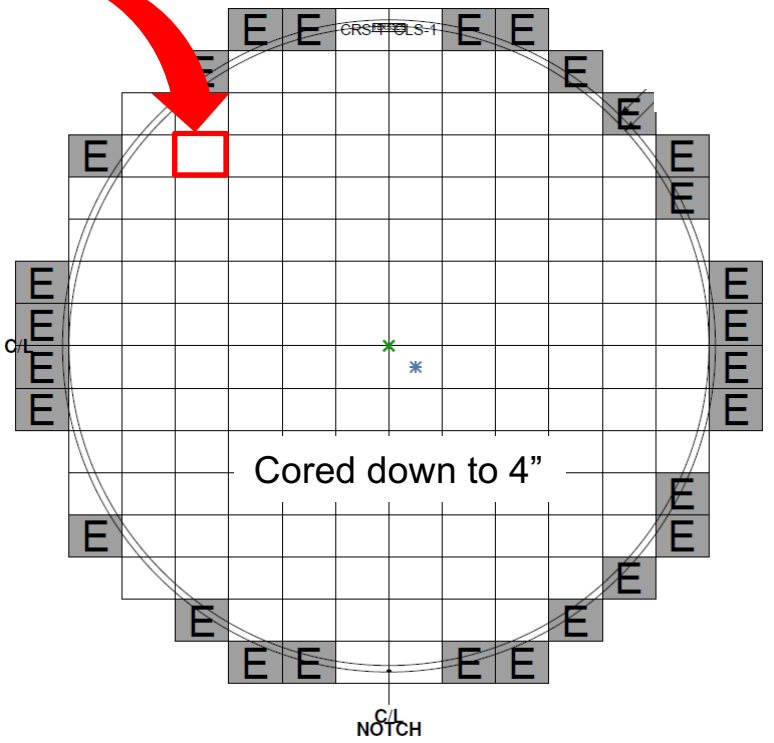


- Metallization on ROIC and Waveguide layer were jointly optimized to enable a closely-spaced tiling arrangement

CMOS Reticle & Dedicated Wafer

Overall Reticle





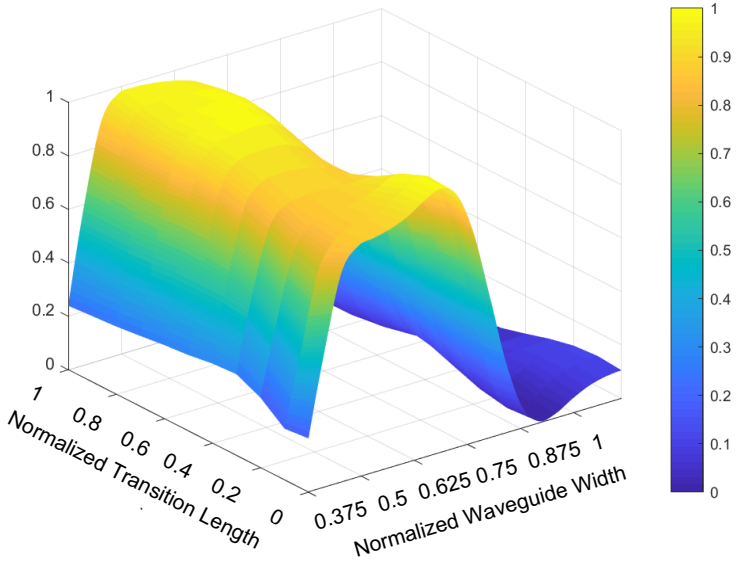
126 full reticles/wafer

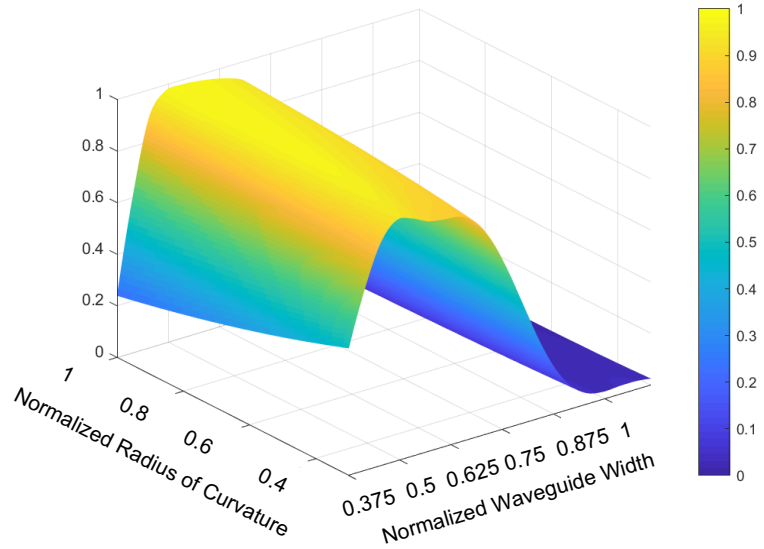
1368 total chips from 2 wafers

Two Digital ROIC Variants are Currently in Fabrication

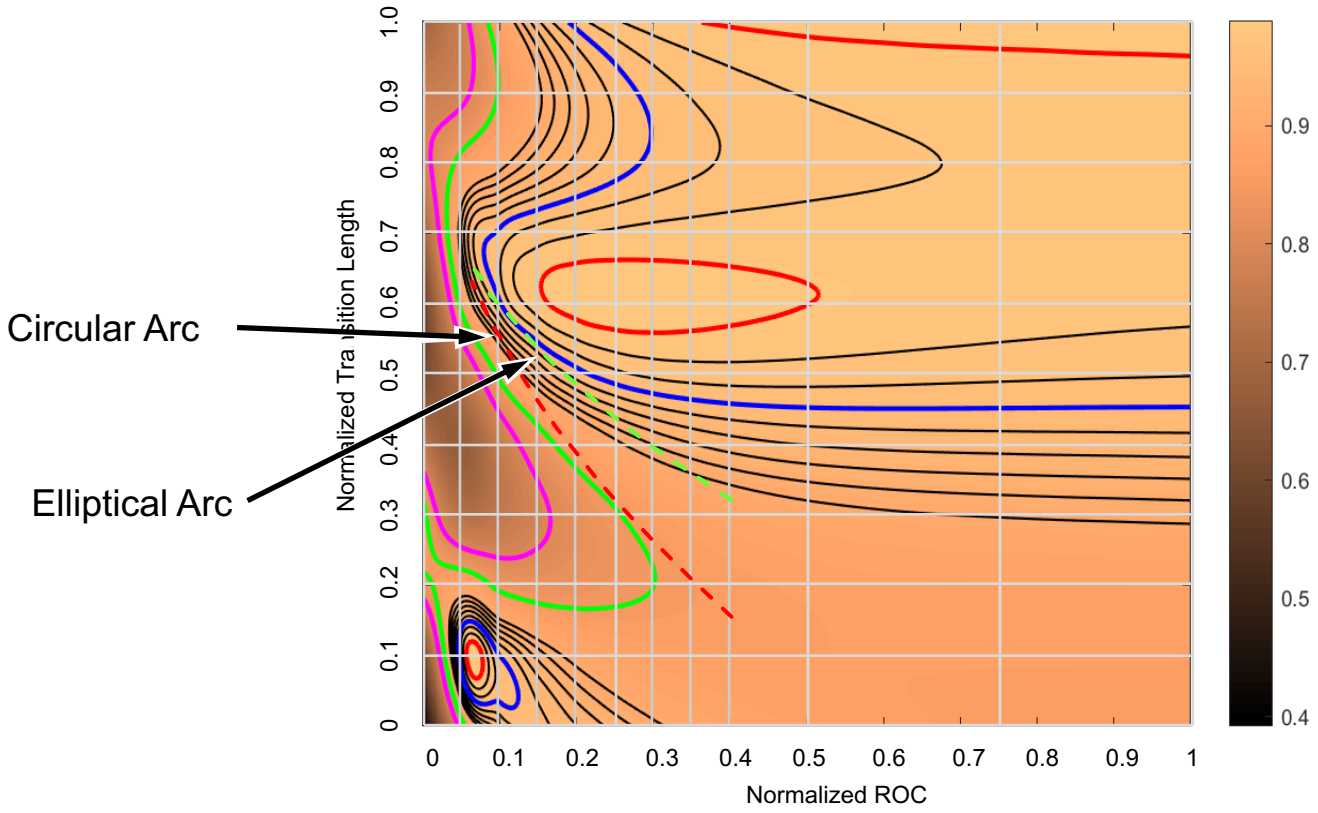
Waveguide Design Optimization

- Waveguide performance impacted by fabrication process limitations
- Current program effort is focused on optimization of waveguide design geometries as driven by fabrication process capabilities
- Completed an extensive model development effort - validated 2-D and 3-D models which are used to test impact of various design parameters on waveguide throughput



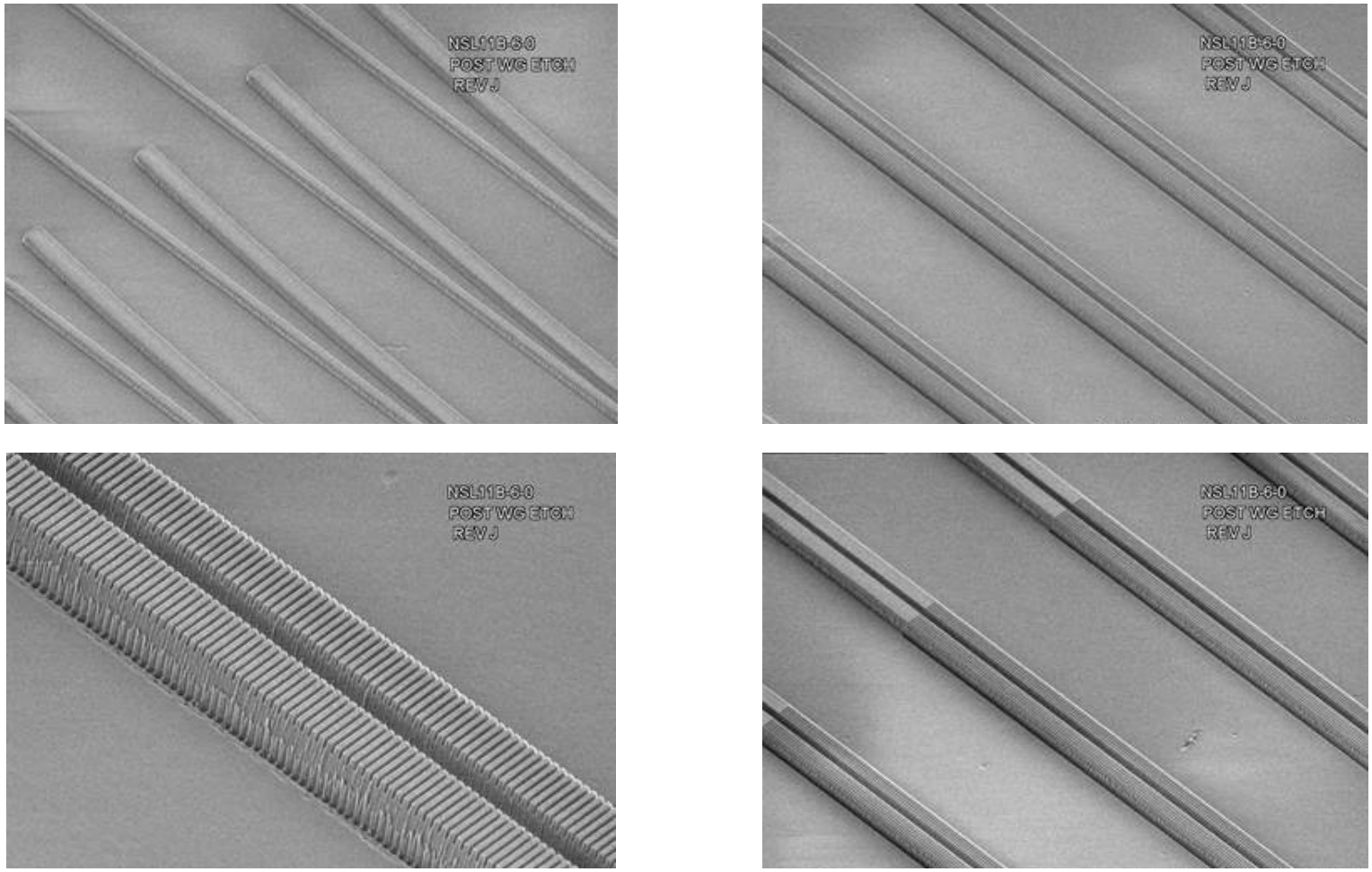


Throughput Comparisons for Waveguide Optimization



Transition Length vs Radius of Curvature : Comparing Circular and Elliptical Merge Geometries for Waveguide Input Arm

Fabrication of Updated Waveguide Near Completion



- New waveguide geometries are being fabricated - optimized to mitigate process limitations

Summary

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- Completed initial prototypes: designed, fabricated, integrated, and tested devices with initial waveguide and detector designs
- Significant progress on fabrication process development
  - Demonstrated numerous successful integrations
  - Optimized etch processes (waveguide and detector)
- Completed ROIC design
  - Unit cells fabricated and tested
  - Final design in fabrication
- Developed validated 3-D waveguide models and carried out extensive design optimization efforts
- Fabricated optimized waveguide geometries – preparing devices for test

Acknowledgement

We would like to thank NASA ESTO for the valuable review, interactions, comments and continued support through SLI-T grant 80NSSC18K0107

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